DETAILED ACTION

*** This office action is in response to Applicant's amendment filed March 06, 2008. Claims 1-10,16-21,25-34 are pending. Claims 11-15 and 22-24 were cancelled by Applicant.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1-5,7-9,16-19,21,27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Nogami (2001/0041447) and Ulrich et al (5,897,379).

Re claim 1, Hongo teaches (at Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45) a method of forming a layer of a conductive material on a wafer, wherein a seed layer coats a front surface and an edge surface of the wafer, and wherein the edge surface includes a back edge surface, a bevel surface and a front edge surface, the method comprising the steps of: removing an edge portion of the seed layer 83 from the back edge surface and the bevel surface without removing the seed layer form a central portion of the front surface and front edge surface; and forming the conductive material 85 onto the seed layer 83 coating the front edge surface and the front surface of the wafer (Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45). Re claim 16, Hongo teaches (at Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45) a method of forming a layer of a conductive material 85 on a wafer comprising a front surface, a back surface and an edge surface, the edge surface including a back edge surface, a bevel surface and a front edge surface, the method comprising the steps of: depositing a seed layer 83 on the front surface and the edge surface of the wafer; removing the seed layer 83 from the back edge surface and the bevel surface; and forming the layer by depositing the conductive material 85 onto the seed layer coating the front edge surface and the front surface (Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45). Re claims 2,17, wherein, as shown in Figs 8,7, removing at least a part of the seed layer 83 from the front edge surface. Re claims 3,18, wherein the wafer is rotated during removing the edge portion of the seed layer 83 (Figs 3,7-8; col 2, line 63 through col 4). Re claims 4,19, applying a process solution is applied onto the back edge surface of the wafer while it is rotated (Fig 3; col 3, line 3 through col 4). Re claims 5,21, wherein the step of removing comprises chemical etching (Figs 7-8,3; col 4, lines 50 through col 5, line 12; col 3, line 45

through col 4). Re claim 7, the wafer is rotated prior to removing the at least a part of the seed layer 83 from the front edge surface (Figs 3,7-8; col 3, lines 3-45; col 2, line 63 through col 4). Re claim 8, wherein a process solution is applied to the at least a part of the seed layer on the front edge surface while the wafer is rotated (Figs 3,7,8; col 3, line 3 through col 4, line 67). Re claim 9, wherein the step of removing the at least a part of the seed layer from the front edge surface comprises chemical etching (Figs 7-8,3; col 4, lines 50 through col 5, line 12; col 3, line 45 through col 4). Re claim 27, wherein forming the conductive material 85 includes contacting the seed layer 83 on the front surface or the front edge surface of the wafer W (Figs 1,2,7-8). Re claim 28, wherein removing the edge portion of the seed layer comprising holding the wafer with a wafer carrier (Figs 3-4, col 3, line 3 through col 4), and wherein forming of the layer comprises holding the wafer with the wafer carrier by using the same apparatus (col 5, lines 14-55; Figs 10-11). Re claim 29, wherein chemical etching comprises directing an etching solution towards the back edge of the wafer (Figs 3-5,7-8; col 4, lines 50 through col 5, line 12; col 3, line 45 through col 4).

Re claim 1, Hongo teaches removing the seed layer 83 from the back edge surface and the bevel after forming the conductive material 85 onto the seed layer 83, whereas, claim 1 recites removing the seed layer from the back edge surface and the bevel surface before forming the conductive material, thereby the central portion of the seed layer is exposed, while claim 16 recites the entire seed layer is exposed.

However, first, Hongo, the primary reference, already teaches at column 1, lines 19-49 that "…as shown in FIG. 1 a barrier layer 80 is formed on the front surface of the wafer…, a Cu seed layer 83 is formed thereon , and a plating layer 85 is formed on the seed layer 83. However,...Cu seed layer 83...is not only on the front surface of the wafer by a thin sputtered Cu layer is Formed also on the edge section E of the wafer as shown in Fig. 2...". Second, Nogami teaches (at Figs 2A-2C; paragraphs 12-21) before plating to form a layer of a conductive copper material on a seed layer, removing an edge portion of the barrier/seed layer (Figs 2A-2C; paragraphs 17-21) from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed/barrier layer on the front surface of the wafer (Fig 2C), without removing the seed layer 116 from a central portion of the front surface and front edge surface while the central portion of the seed layer 116 is exposed (Fig 2B), and

wherein the entire seed layer 116 is exposed (Fig 2B); and then forming a conductive material on the seed/barrier layer 116,114 after removing of the seed/barrier layer 116/114 (Figs 2A-2C; paragraphs 17-21) from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface. Ulrich teaches an selective etching process for selectively removing an edge portion of the seed conductive layer 32 from the back edge surface and the bevel surface without removing the seed conductive layer 32 from the central portion of the front surface while the central portion of the seed conductive layer 32 is exposed and while the entire seed conductive layer 32 is exposed, wherein removing the edge portion of the seed conductive layer 32 is alternatively performed by an etching process without the use of a photoresist 42 as a masking layer (Figs 9-12; col 7, line 22 to col 8; and Figs 4-6; col 6, line 11 to col 7). Additionally, Hongo also already teaches (at Figs 4-6; col 3, line 45 to col 4, ; Figs 7,8; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45) an etching process and apparatus (Figs 4-7) for selectively removing the edge portion of the seed layer 83 from the back edge surface and the bevel surface without removing the seed layer 83 from the central portion of the front surface and front edge surface, wherein an edge portion of the conductive layer 85 is also selectively removed without removing the conductive layer 85 from the central portion of the front surface and front edge surface while the central portion of the top conductive layer 85 is exposed and while the entire conductive layer 85 is exposed (Figs 7,8; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45).

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made before forming a layer of the conductive material on the seed layer of Hongo by removing the edge portion of the seed layers including the barrier seed layer and the seed layer from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed layers on the central portion of the front surface of the wafer, without removing the seed layer from a central portion of the front surface and front edge surface while the central portion of the top seed layer is entirely exposed, as taught by Nogami, Ulrich et al, and Hongo. This is because of the desirability to prevent forming the conductive material at unwanted edge surface, and because of the desirability to deposit the conductive material at a selected portion on the seed layer at the front surface of the wafer so that the step of removing the conductive material at the edge surfaces after depositing

the conductive material is not necessarily needed, thereby reducing processing steps. This is also because of the desirability to provide copper interconnects with reduced contamination due to copper deposited at the edge or rear of the substrate (Nogami, paragraphs 21,20).

2. Claims 6,10,20,30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Nogami (2001/0041447) and Ulrich et al (5,897,379), as applied to claims 1-5,7-9,16-19,21,27-29 above, and further of Volodarsky et al (6,352,623).

The references including Hongo, Nogami, and Ulrich teach a method for forming a conductive layer as applied to claims 1-5,7-9,16-19,21,27-29 above.

The references including Hongo already teaches removing the seed layer by chemical etching, wherein the edge of the wafer is inserted into a cavity (Figs 4-5, re claim 33).

Claims 6,10 and 20 recite removing the seed layer by electrochemical etching, and by contacting the wafer with porous media (re claim 32), and rotating the wafer (claim 34).

However, Volodarsky teaches (at Figs 1-2; col 5, lines 8-27, col 4) employing an ECMD process and apparatus for depositing and removing a layer by electrochemical etching or chemical etching, wherein the electrochemical etching comprises contacting the wafer with porous media pad 24 (Fig 1, col 4, lines 45-67, re further claim 32), and wherein the wafer is rotated (Fig 1, col 4, lines 28-67, re claim 34) up to 200 rpm (col 8, lines 13-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the layer of Hongo by employing the ECMD process for removing a layer by electrochemical etching or chemical etching as taught by Volodarsky. This is because electrochemical etching and chemical etching are alternative and art recognized equivalent etching process for removing a portion of the layer from the wafer, wherein the electrochemical etching is an effective process for removing a layer in a reliable manner.

Re claims 30-31, Volodarsky teaches (at col 8, lines 13-25; Fig 1, col 4, lines 28-67) rotating the wafer up to 200 rpm during the etching. Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of rotation of the wafer, as taught by Volodarsky, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable

modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

3. Claims 25,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Nogami (2001/0041447) and Ulrich et al (5,897,379) as applied to claims 1-5,7-9,16-19,21,27-29 above, and further of the same Ulrich et al (5,897,379).

The references of Hongo, Nogami, and Ulrich teach a method for forming a conductive layer as applied to claims 1-5,7-9,16-19,21,27-29 above.

Claims 25-26 recite removing at least part of the seed layer from the front edge surface after forming the conductive material layer.

However, Hongo teaches (at Figs 7-8; col 4, line 50 through col 6) removing at least part of the seed layer from the front edge surface after forming the conductive material layer 85. Ulrich also teaches (at Figs 3-5; col 5, line 56 through col 6; Figs 9-11; col 7, lines 22-50; cols 1-2) patterning and removing at least a part of a portion of the conductive layer 32 after forming the conductive material layer 32 in order to form interconnect lines for the integrated circuit (IC).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to continue the semiconductor fabrication of the references including Hongo by patterning and removing a portion of the conductive material layer and a part of the seed layer after forming the conductive material layer, as taught by Ulrich and Hongo. This is because of the desirability to remove the unwanted conductive material layer from the perimeter of the wafer, and because of the desirability to pattern the conductive material layer in order to form an electrical interconnection for an semiconductor device.

Response to Amendment

4. Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant remarked (at 3/6/08 remark page 7) that "…Nogami does not teach or suggest that the seed layer 116 is formed on the bevel surface and the back edge surface…".

In response, in the combination of the references including Hongo as a primary reference, in which Hongo clearly discloses at column 1, lines 19-49 that "…as shown in FIG. 1 a barrier layer 80 is formed on the front surface of the wafer…, a Cu seed layer 83 is formed thereon , and a plating layer 85 is formed on the seed layer 83. However,...Cu seed layer 83...is not only on the front surface of the wafer but a thin sputtered Cu layer is formed also on the edge section E of the wafer as shown in Fig. 2...". Thus one of ordinary skill in the art would have recognized and obviously to realize the teachings of Hongo to Nogami in that the seed layer 116 is not only on the front surface of the wafer but is also on the edge section the wafer. Moreover, Hongo is a primary references expressly discloses the seed layer 83 and the barrier layer 80 are both formed on the front surface and an edge surface of the wafer, and wherein the edge surface includes a back edge surface, a bevel surface, and a front edge surface, wherein an edge portion of the conductive layer 85 is also selectively removed without removing the central portion of the conductive layer while the central portion of the conductive layer 85 is exposed and while the entire conductive layer 85 is exposed during this selective etching by applying etching liquid to the edge portion only while rotating of the wafer.

In the combination of the references, Nogami clearly teaches, **before** plating a conductive material on the seed layer, removing an edge portion of the seed layer from the back edge surface and the bevel surface without removing the seed layer form a central portion of the front surface and front edge surface. Ulrich and Hongo prima facie teaches an etching process and apparatus for one of ordinary skill in the art to employ in order to selectively remove an edge portion of the top conductive layer while the central portion of the top conductive layer is exposed.

The rejection is outstanding and one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (571) 273-8300.

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Oacs-24-1

/Michael Trinh/

Primary Examiner, Art Unit 2822